AMENDMENTS TO THE CLAIMS

1-21 (cancelled).

22. (original) A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a polysilicon layer provided on said gate oxide layer;

at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

23. (original) A structure as in claim 22, further comprising first sidewall spacers on sidewalls of said gate stack.

24. (original) A structure as in claim 23, further comprising second sidewall spacers provided over and at edges of said conducting layer.

25. (original) A structure as in claim 23, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers.

26. (original) A structure as in claim 24, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

27. (original) A structure as in claim 23, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

28. (original) A structure as in claim 27, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

29. (original) A structure as in claim 25, further comprising second sidewall spacers provided over and at edges of said conducting layer.

30. (original) A structure as in claim 29, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

31. (original) A structure as in claim 25, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

32. (original) A structure as in claim 31, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

33. (original) A structure as in claim 22, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

34. (original) A system comprising:

a processor; and

a memory device coupled to said processor, at least one of said processor and said memory device comprising a transistor structure, said transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a polysilicon layer provided on said gate oxide layer;

at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

35. (original) A structure as in claim 34, further comprising first sidewall spacers on sidewalls of said gate stack.

36. (original) A system as in claim 35, further comprising second sidewall spacers provided over and at edges of said conducting layer.

37. (original) A system as in claim 35, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers.

38. (original) A system as in claim 36, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

39. (original) A system as in claim 35, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

40. (original) A system as in claim 39, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

41. (original) A system as in claim 37, further comprising second sidewall spacers provided over and at edges of said conducting layer.

42. (original) A system as in claim 41, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

43. (original) A system as in claim 37, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

44. (original) A system as in claim 43, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

45. (original) A system as in claim 34, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and combinations thereof.

Claims 46-63 (cancelled).

64. (original) A gate stack structure provided on a semiconductor substrate comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers on sidewalls of said gate stack;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers;

second sidewall spacers provided over and at edges of said conducting layer;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers

at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

65. (original) A structure as in claim 64, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

66. (original) A structure as in claim 65, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

67. (original) A structure as in claim 64, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

68. (original) A structure as in claim 67, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

69. (original) A structure as in claim 64, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

70. (original) A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers;

at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

71. (original) A structure as in claim 70, wherein said conducting layer is polysilicon.

72. (original) A structure as in claim 70, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

73. (original) A structure as in claim 72, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

74. (original) A structure as in claim 70, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

75. (original) A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

second sidewall spacers provided over and at edges of said conducting layer;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers;

at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

76. (original) A structure as in claim 75, wherein said conducting layer is polysilicon.

77. (original) A structure as in claim 75, further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack.

78. (original) A structure as in claim 77, further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area.

79. (original) A structure as in claim 77, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

80. (original) A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

an insulating layer adjacent to said first sidewall spacers, said insulating layer and said sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area;

at least one unetched silicide layer formed over and in contact with said conducting layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

81. (original) A structure as in claim 80, wherein said conducting layer is polysilicon.

82. (original) A structure as in claim 80, further comprising second sidewall spacers provided over and at edges of said conducting layer.

83. (original) A structure as in claim 82, further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers.

84. (original) A structure as in claim 80, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

85. (original) A transistor structure comprising:

a semiconductor substrate;

a gate stack provided over said substrate, said gate stack comprising:

a gate oxide layer provided on said substrate;

a conducting layer provided on said gate oxide layer;

first sidewall spacers provided on sidewalls of said gate stack;

an insulating layer adjacent to said first sidewall spacers, said insulating layer and said sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack;

second sidewall spacers provided over and at edges of said conducting layer;

at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers;

at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

86. (original) A structure as in claim 85, wherein said silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and combinations thereof.

87. (original) A method of fabricating a gate structure of a transistor, said method comprising:

forming an oxide layer over a substrate;

forming a conducting layer over said oxide layer;

forming an insulating layer over said conducting layer;

removing portions of said oxide layer, said conducting layer, and said insulating layer to form a gate stack, said gate stack having an oxide layer, a conducting layer, and an insulating layer;

removing said insulating layer from said gate stack to expose said conducting layer; and,

providing a metal-containing layer on said exposed conducting layer which can form a silicide.

88. (original) A method as in claim 87, wherein said conducting layer comprises a polysilicon layer.

89. (original) A method as in claim 87, wherein said step of forming said silicide further comprises providing at least one unetched metal-containing layer over said exposed conducting layer and processing said unetched metal-containing layer and conducting layer to form said silicide layer.

90. (original) A method as in claim 87, wherein said metal-containing layer is an unetched metal layer.

91. (original) A method as in claim 90, wherein said unetched metal layer contains a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.